NEC

Application Note

V850ES/Jx3-L

Sample Program (Watchdog Timer 2 (WDT2))

Reset Generated by Infinite Loop Detection

This document summarizes the operations of the sample program and describes how to use the sample program and how to set and use watchdog timer 2. In the sample program, an interrupt is generated by detecting the falling edge of the switch input. If no WDT2 overflow occurs, LED1 blinks in a cycle of approximately 55 ms while SW1 is turned on. After SW1 is turned off, LED1 blinks in a cycle of approximately 120 ms. If a WDT2 overflow occurs, a reset signal is generated by WDT2. After the reset is released, LED2 is turned on and LED1 blinks in a cycle of approximately 120 ms.

Target devices

V850ES/JF3-L microcontroller
V850ES/JG3-L microcontroller

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CHAPTER 1 OVERVIEW

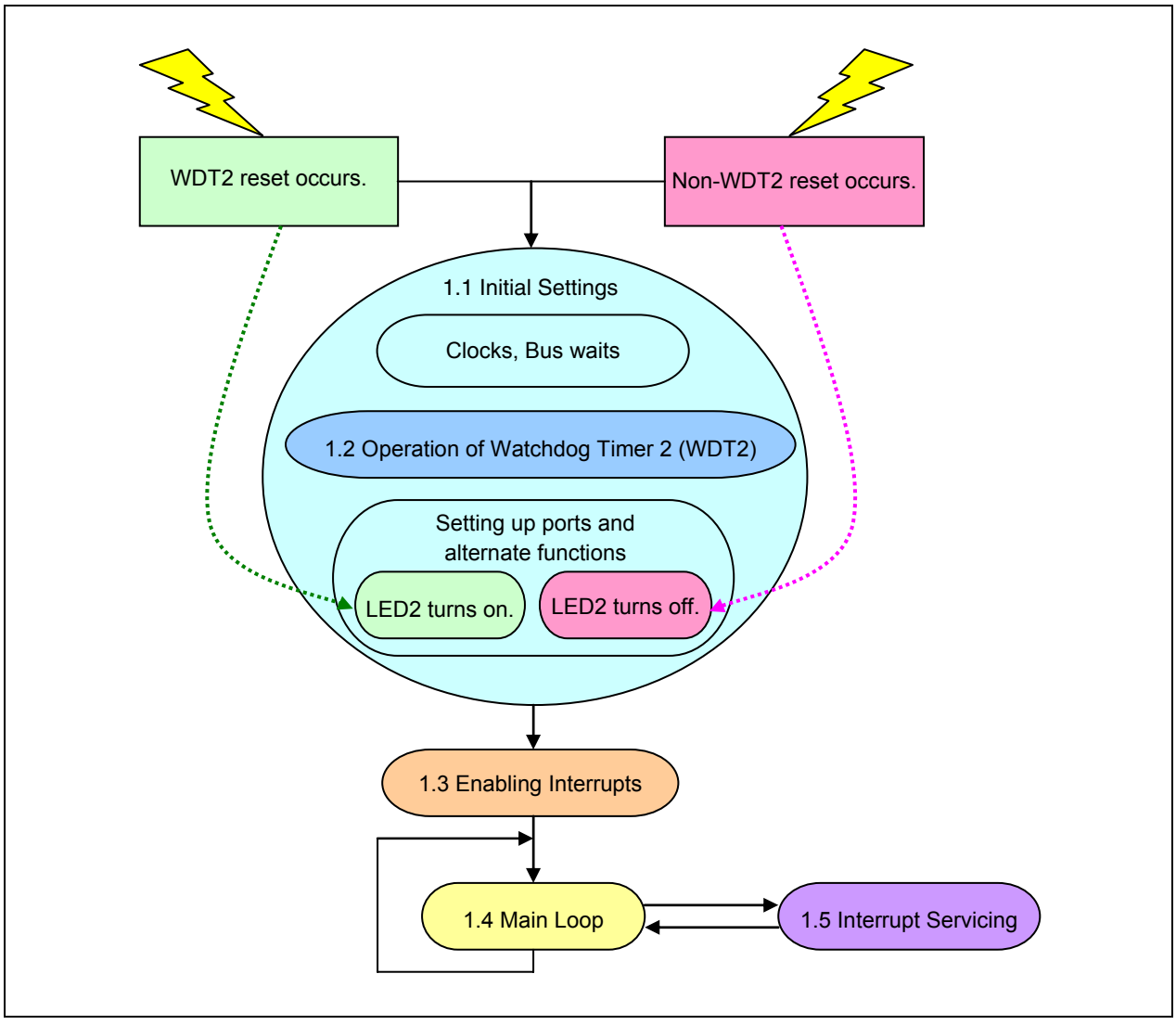
This sample program describes the usage of watchdog timer 2 (WDT2).

The overflow time of WDT2 is specified as 125 ms based on the subclock. When an overflow occurs, an internal reset signal (WDT2RES) is generated.

After initial setup is complete, an interrupt is generated and serviced when the falling edge of the switch input is detected. LED1 blinks and the WDT2 counter is cleared in a cycle of 55 ms while the switch is being pressed. When a reset is generated by WDT2, the initial settings specify that LED2 turns on.

The settings for peripheral functions that remain stopped after reset is released and that are not used in this sample program have not been specified.

The main software operations are shown below.



1.1 Initial Settings

<Referencing option byte>
- Referencing the oscillation stabilization time after releasing reset

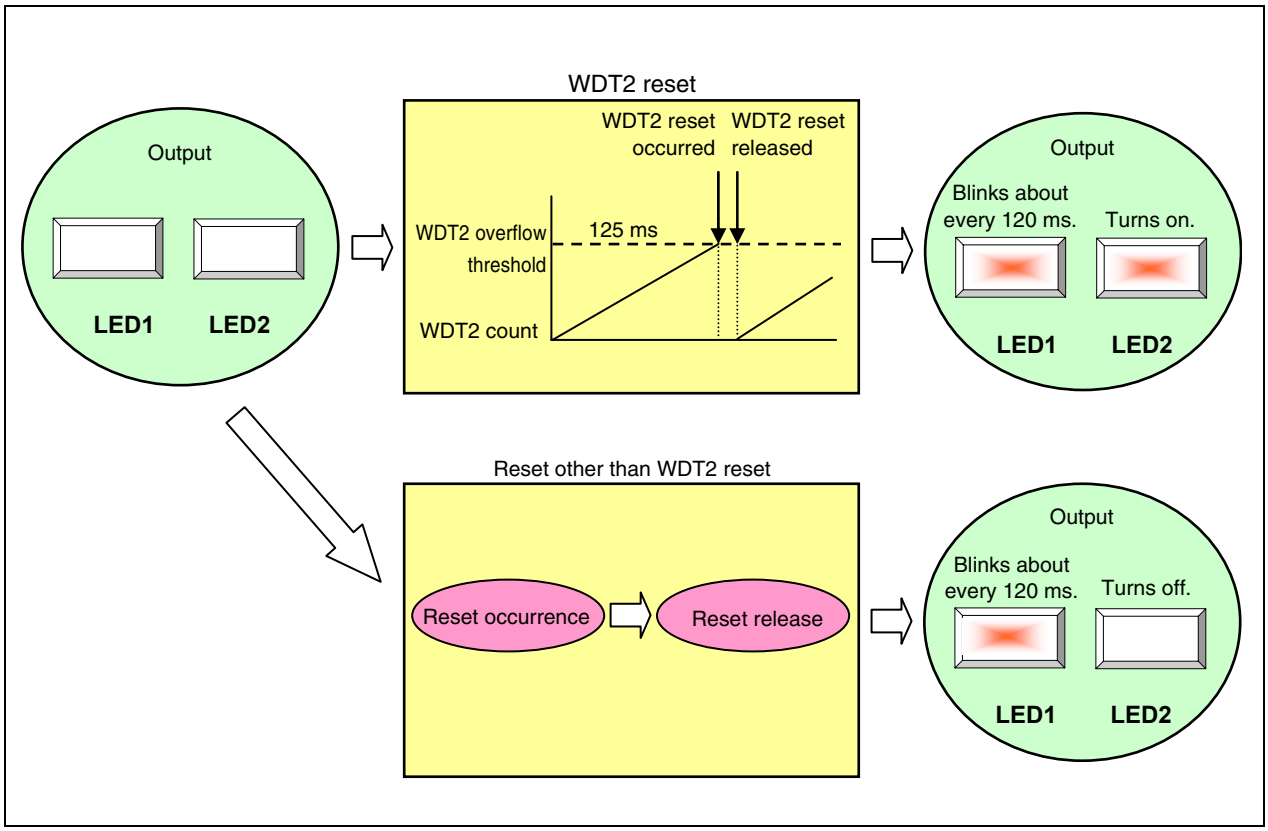
<Settings of on-chip peripheral functions>
- Setting wait operations <wait: 1> for bus access to on-chip peripheral I/O registers
- Setting on-chip debug mode <normal operation mode>
- Stopping the internal oscillator, setting watchdog timer 2 mode <reset mode>
- Setting the use of the subclock and setting the internal system clock
- Setting to PLL mode and setting to 20 MHz operation (5 MHz × 4).

<Pin settings>
- Setting unused pins
- Setting external interrupt pins (edge specification, priority specification, unmasking)
- Setting LED output pins

<Settings of 16-bit interval timer M (TMM)>
- Selecting the count clock (fxx/512)
- Setting the TMM count
- Masking interrupts from timer M
- Enabling operation of TMM

1.2 Operation of Watchdog Timer 2 (WDT2)

Watchdog timer 2 generates an internal reset signal (WDT2RES) when an overflow occurs.
When a WDT2 reset occurs, LED2 turns on and LED1 blinks about every 120 ms.
When a reset other than a WDT2 reset occurs, LED2 turns off and LED1 blinks about every 120 ms.



1.3 Enabling Interrupts

- Enabling interrupts by using the EI instruction

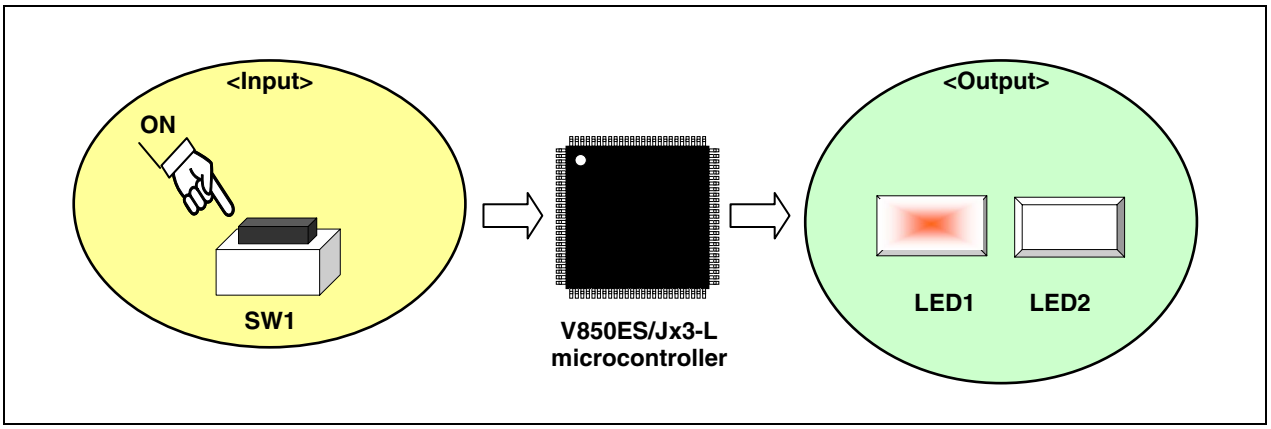
1.4 Main Loop

- Executing an infinite loop (LED1 blinks about every 120 ms while the system is waiting for an interrupt generated by switch input.)

1.5 Interrupt Servicing

Interrupts are serviced by detecting the falling edge of the INTP0 pin, caused by switch input. In interrupt servicing, the LED1 blinking cycle is changed by confirming that the switch is on, after about 10 ms have elapsed after the falling edge of the INTP0 pin was detected.

The switch being off, after about 10 ms have elapsed after the falling edge of the INTP0 pin was detected, is identified as chattering noise and the LED1 blinking cycle is not changed.



The reset source is confirmed (RESF = 0x00).
→ LED1 blinks (120 ms), LED2 turns off.
→ A switch input interrupt occurs.
→ LED1 blinks (55 ms).
→ A reset occurs triggered by a WDT2 overflow.
→ The reset source is confirmed (RESF = 0x10).
→ LED2 turns on, LED1 blinks (120 ms)

Caution See each product user's manual (V850ES/Jx3-L) for cautions when using the device.

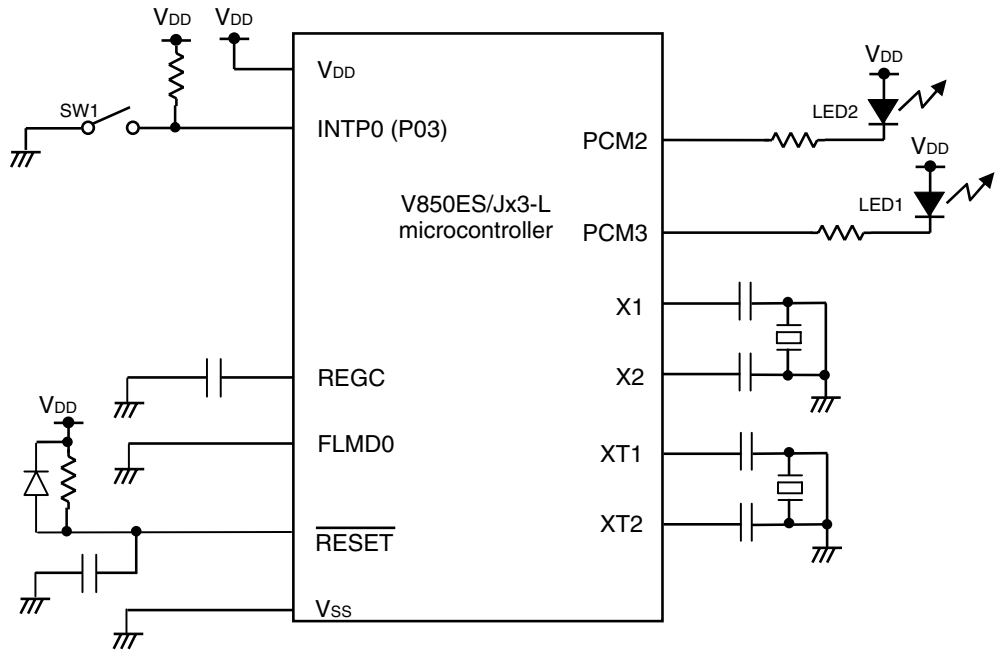
[Column] What is chattering?
Chattering is a phenomenon that an electric signal alternates between being on and off when a connection flip-flops mechanically immediately after a switch is switched.

CHAPTER 2 CIRCUIT DIAGRAM

This chapter describes a circuit diagram and the peripheral hardware to be used in this sample program.

2.1 Circuit Diagram

The circuit diagram is shown below.



Cautions 1. Connect the EV_{DD}, AV_{REF0}, and AV_{REF1} pins directly to V_{DD}.

2. Connect the EV_{SS} and AV_{SS} pins directly to GND.

3. Connect the FLMD0 pin to GND in normal mode.

4. Connect REGC to GND via a capacitor (recommended value: 4.7 μF).

5. Leave all unused ports open, because they will be handled as output ports.

2.2 Peripheral Hardware

The peripheral hardware to be used is shown below.

(1) Switch (SW1)

This switch is used as an interrupt input to control the lighting of LED1.

(2) LEDs (LED1, LED2)

LED1 is used as outputs corresponding to switch inputs.

When a reset signal is generated by watchdog timer 2, LED2 turns on following reset release.

CHAPTER 3 SOFTWARE

This chapter describes the file configuration of the compressed files to be downloaded, on-chip peripheral functions of the microcontroller to be used, and the initial settings and an operation overview of the sample program. A flowchart is also shown.

3.1 File Configuration

The following table shows the file configuration of the compressed files to be downloaded.

File Name (Tree Structure)	Description	Compressed (*.zip) Files Included	
c / conf / crtE.s	Startup routine file[Note 1]	–	●
c / conf / AppNote_WDT2.dir	Link directive file[Note 2]	●	●
c / conf / AppNote_WDT2.prj	Project file for integrated development environment PM+	–	●
c / conf / AppNote_WDT2.prw	Workspace file for integrated development environment PM+	–	●
c / src / main.c	C language source file including descriptions of hardware initialization processing and main processing of microcontroller	●	●
c / src / minicube2.s	Source file for reserving area for MINICUBE2	●	●
c / src / opt_b.s	Source file for setting option byte	●	●

Notes 1. This is the startup file copied when “Copy sample for use (C)” is selected when “Specify startup file” is selected when creating a new workspace. (If the default installation path is used, the startup file will be a copy of C:\Program Files\NEC Electronics Tools\PM+*Version used*\lib850\r32\crtE.s.)

2. This is the link directive file automatically generated when “Copy sample for use (C)” is selected and “Memory usage: Internal memory only (I)” is checked when “Specify link directive file” is selected when creating a new workspace, and to which a segment for MINICUBE2 is added. (If the default installation path is used, C:\Program Files\NEC Electronics Tools\PM+*Version used*\bin\w_data\V850_i.dat is used as the reference file.)

Remark : Only the source file is included.

: The files to be used with integrated development environment PM+ are included.

3.2 On-Chip Peripheral Functions Used

The following on-chip peripheral functions of the microcontroller are used in this sample program.

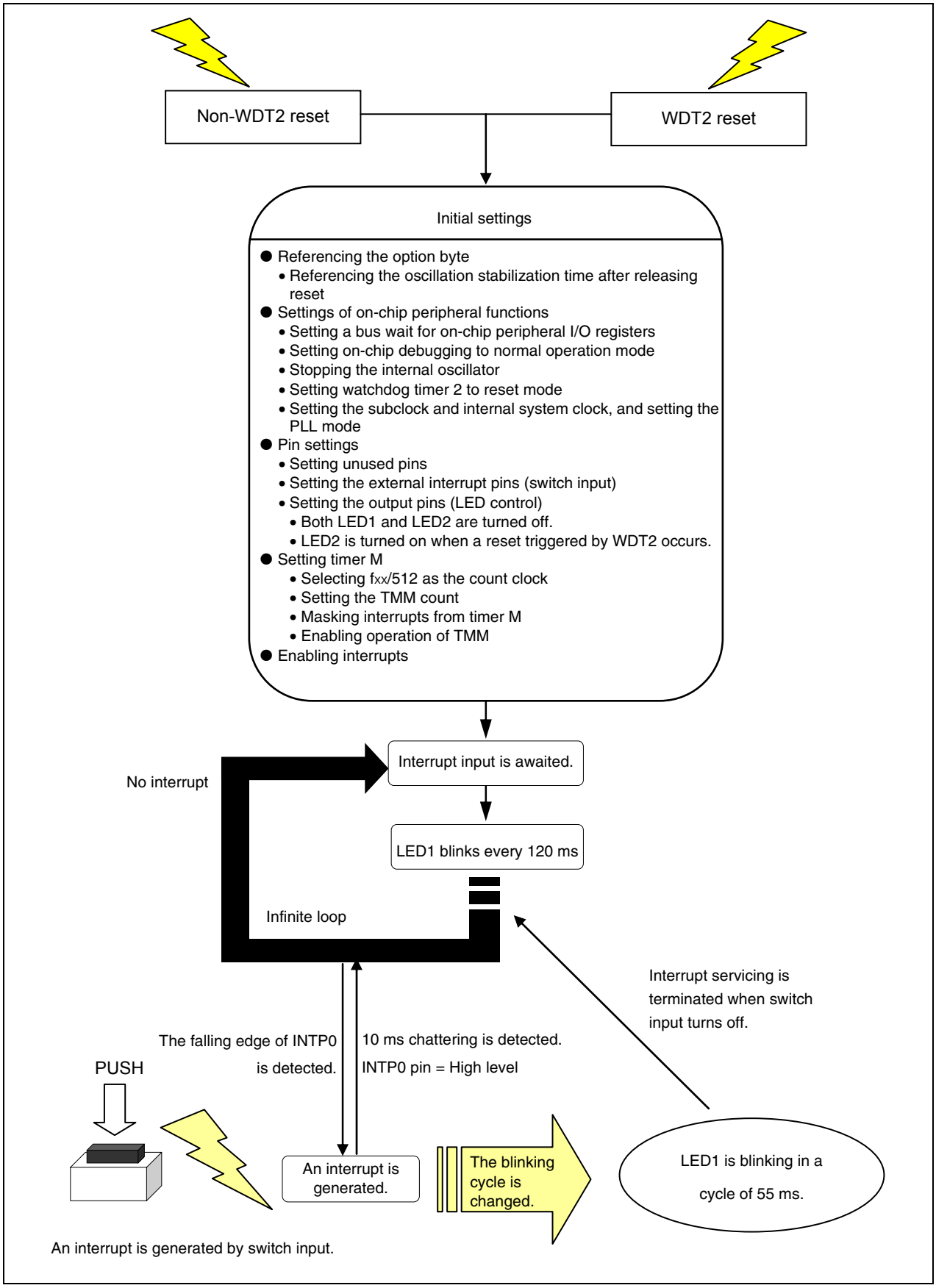
- Watchdog timer 2 (used to generate an overflow): WDT2
- 16-bit interval timer M (used to generate the LED blinking cycle): TMM
- External interrupt input (for switch input): INTP0 (SW1)
- Output ports (for lighting LEDs): PCM2 (LED2), PCM3 (LED1)

3.3 Initial Settings and Operation Overview

In this sample program, the selection of the clock frequency, setting of WDT2, setting of the I/O ports and external interrupt pins, setting of a TMM count clock, setting of interrupts, and ROMization processing are performed in the initial settings.

After initial setup is complete, LED1 blinks about every 120 ms, and interrupts are generated and serviced upon detection of the falling edge of the switch input (SW1). If no WDT2 overflow occurs during interrupt servicing, LED1 blinks about every 55 ms while SW1 is turned on. When SW1 is turned off, LED1 blinks about every 120 ms. If a WDT2 overflow occurs during interrupt servicing, watchdog timer 2 generates a reset signal. After the reset is released, LED2 turns on and LED1 blinks about every 120 ms.

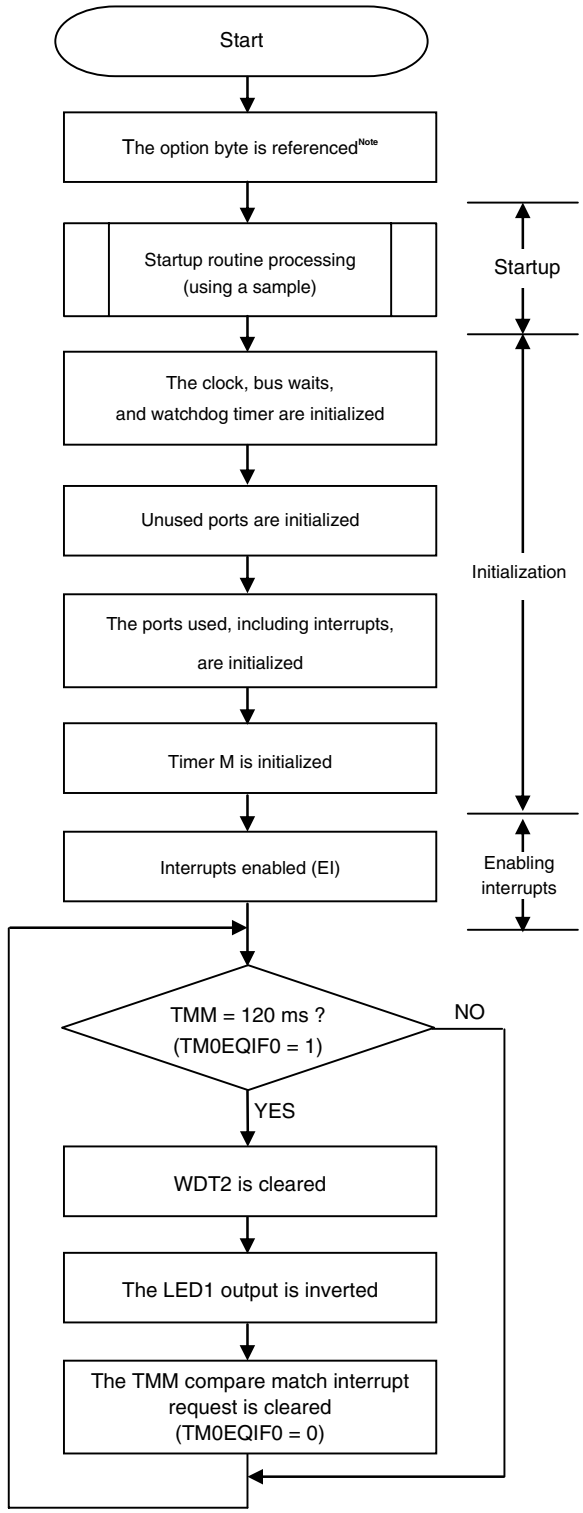
The details are described in the state transition diagram shown below.


Non-WDT2 reset
WDT2 reset
Initial settings
● Referencing the option byte
• Referencing the oscillation stabilization time after releasing reset
● Settings of on-chip peripheral functions
• Setting a bus wait for on-chip peripheral I/O registers
• Setting on-chip debugging to normal operation mode
• Stopping the internal oscillator
• Setting watchdog timer 2 to reset mode
• Setting the subclock and internal system clock, and setting the PLL mode
● Pin settings
• Setting unused pins
• Setting the external interrupt pins (switch input)
• Setting the output pins (LED control)
• Both LED1 and LED2 are turned off.
• LED2 is turned on when a reset triggered by WDT2 occurs.
● Setting timer M
• Selecting fxx/512 as the count clock
• Setting the TMM count
• Masking interrupts from timer M
• Enabling operation of TMM
● Enabling interrupts
Interrupt input is awaited.
No interrupt
LED1 blinks every 120 ms
Infinite loop
Interrupt servicing is terminated when switch input turns off.
The falling edge of INTP0 is detected.
10 ms chattering is detected.
INTP0 pin = High level
PUSH
An interrupt is generated.
The blinking cycle is changed.
LED1 is blinking in a cycle of 55 ms.
An interrupt is generated by switch input.

3.4 Flowchart

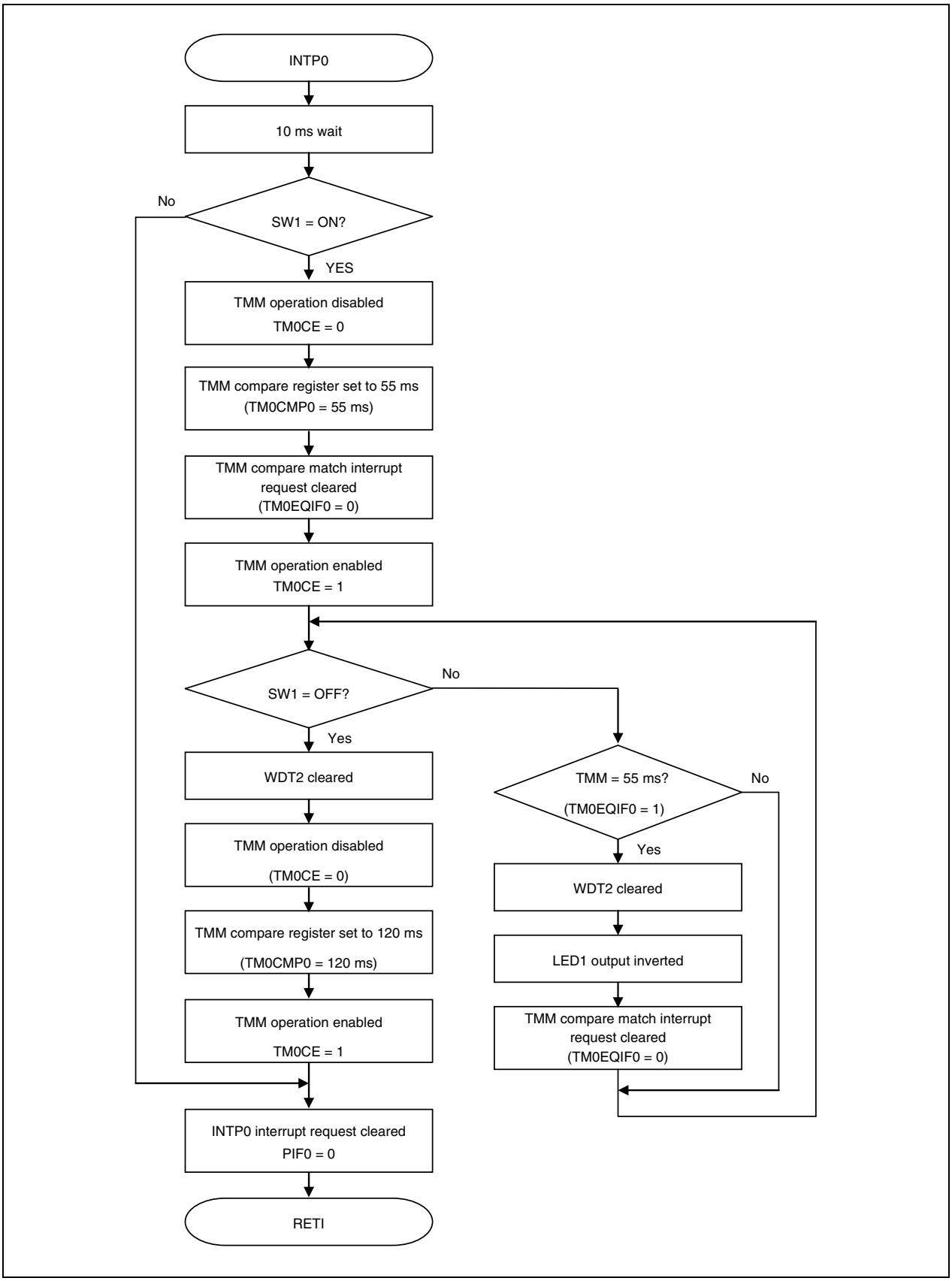
A flowchart for the sample program is shown below.

• Main processing flow


Start
The option byte is referenced Note
Startup routine processing (using a sample)
Startup
The clock, bus waits, and watchdog timer are initialized
Unused ports are initialized
Initialization
The ports used, including interrupts, are initialized
Timer M is initialized
Interrupts enabled (EI)
Enabling interrupts
TMM = 120 ms ? (TM0EQIF0 = 1)
NO
YES
WDT2 is cleared
The LED1 output is inverted
The TMM compare match interrupt request is cleared (TM0EQIF0 = 0)

Note The option byte is automatically referenced by the microcontroller after reset is released. In this sample program, the oscillation stabilization time after releasing reset is set to 6.554 ms with the option byte.

• Interrupt servicing flow



[Column] Contents of the startup routine

The startup routine is a routine that is executed before executing the main function after reset of the V850 is released. Basically, the startup routine executes initialization so that the program written in C language can start operating.

Specifically, the following are performed.

- Securing the argument area of the main function
- Securing the stack area
- Setting the RESET handler when reset is issued
- Setting the text pointer (tp)
- Setting the global pointer (gp)
- Setting the stack pointer (sp)
- Setting the element pointer (ep)
- Setting mask values to the mask registers (r20 and r21)
- Clearing the sbss and bss areas to 0
- Setting the CTBP value for the prologue epilogue runtime library of the function
- Setting r6 and r7 as arguments of the main function
- Branching to the main function

3.5 Differences Between V850ES/JG3-L and V850ES/JF3-L

The V850ES/JG3-L is the V850ES/JF3-L with its functions, such as I/Os, timer/counters, and serial interfaces, expanded.

In this sample program, the initialization range of P1, P3, P7, P9, and PDH in I/O initialization differs.

See **APPENDIX A PROGRAM LIST** for details of the sample program.

3.6 Security ID

The content of the flash memory can be protected from unauthorized reading by using a 10-byte ID code for authorization when executing on-chip debugging using an on-chip debug emulator.

For details of ID security, see the **V850ES/Jx3-L Sample Program (Interrupt) External Interrupt Generated by Switch Input Application Note**.

CHAPTER 4 SETTING REGISTERS

This chapter describes the watchdog timer 2 (WDT2) settings.

For other initial settings, refer to the **V850ES/Jx3-L Sample Program (Initial Settings) LED Lighting Switch Control Application Note**. For interrupt, refer to the **V850ES/Jx3-L Sample Program (Interrupt) External Interrupt Generated by Switch Input Application Note**.

Among the peripheral functions that are stopped after reset is released, those that are not used in this sample program are not set.

For how to set registers, see each product user's manual.

- V850ES/JG3-L 32-bit Single-Chip Microcontroller
  Hardware User's Manual
- V850ES/JF3-L 32-bit Single-Chip Microcontroller
  Hardware User's Manual

See the following user's manuals for details of extended descriptions in C and assembly languages.

- CA850 C Compiler Package C Language User's Manual
- CA850 C Compiler Package Assembly Language User's Manual

4.1 Settings of Watchdog Timer 2 (WDT2)

Watchdog timer 2 operates in the following two modes:

- A mode in which WDT2 is used as a reset trigger
- A mode in which WDT2 is used as an interrupt trigger

Watchdog timer 2 is mainly controlled by the following two registers:

- Watchdog timer mode register 2 (WDTM2)
- Watchdog timer enable register (WDTE)

4.1.1 Watchdog timer mode register 2 (WDTM2)

Watchdog timer mode register 2 (WDTM2) is used to set the overflow time and operating clock of watchdog timer 2.

WDTM2 can be read and written in 8-bit units. This register can be read any number of times, but it can be written only once following reset release.

Reset sets this register to 0x67.

Caution Accessing the WDTM2 register is prohibited in the following statuses.

- **When the CPU is operating on the subclock and main clock oscillation is stopped.**
- **When the CPU is operating on the internal oscillation clock.**

Figure 4-1. Format of WDTM2 Register

Watchdog timer mode register 2 (WDTM2)

Address: 0xFFFF6D0

7	6	5	4	3	2	1	0
0	WDM21	WDM20	WDCS24	WDCS23	WDCS22	WDCS21	WDCS20

WDM21	WDM20	Selection of watchdog timer 2 operation mode
0	0	Operation stopped
0	1	Non-maskable interrupt request mode (WDT2 generates the INTWDT2 signal)
1	×Note	Reset mode (WDT2 generates the WDT2RES signal)

WDCS24	WDCS23	WDCS22	WDCS21	WDCS20	Selection of watchdog timer 2 clock
1	×Note	0	1	1	$2^{12}/f_{XT}$ (125 ms)

Note Either 0 or 1

Remark • The red values in the table indicate the values set in the sample program (WDTM2 = 0x5B).

• f_{XT} = 32.768 kHz

4.1.2 Watchdog timer enable register (WDTE)

Writing 0xAC to the WDTE register clears the counter of watchdog timer 2 and causes the counter to start counting up again.

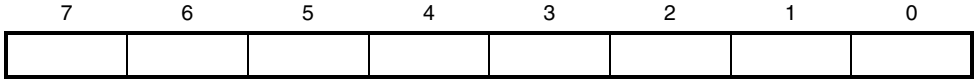
This register can be read and written in 8-bit units. Writing WDTE using a 1-bit memory manipulation instruction will cause an overflow to occur.

Reset sets this register to 0x9A.

Figure 4-2. Format of WDTE Register

Watchdog timer enable register (WDTE)

Address: 0xFFFFF6D1



Cautions 1. Writing a value other than 0xAC to the WDTE register will trigger forcible generation of the overflow signal.

2. To deliberately trigger generation of the overflow signal, write a value other than 0xAC to the WDTE register once, or write to the WDTM2 register twice. Note, however, that if operation of watchdog timer 2 has been stopped, writing a value other than 0xAC to the WDTE register once or writing to the WDTM2 register twice will not trigger generation of the overflow signal.

3. The value read from the WDTE register is 0x9A (which differs from the value written—0xAC).

- Using the detection of a watchdog timer 2 overflow as a trigger to generate a reset
  (Same contents as sample program)

- Setup procedure
  Set WDTM2 to 0x5B (in the program example, this sets reset mode and an operating clock of 212/f_{XT} (125 ms)).
  Set WDTE to 0xAC before the overflow detection time elapses (clearing the watchdog timer 2 count value) to stop the occurrence of a reset. If the watchdog timer 2 count value is not cleared before the overflow detection time elapses, a reset will occur.
  In the program example, the operating clock is set to 212/f_{XT}, so the overflow detection time of watchdog timer 2 is 125 ms.

- Program example (same contents as sample program)

```
#define VAL_120ms_CNT  (4688)       /* Cycle in which WDT2 count is cleared (120 ms)   */
```

Section of initialization processing

Initialization processing for other than WDT2 is omitted here

```
/* Using detection of WDT2 overflow as a reset trigger */
WDTM2 = 0x5B;                   /* Starts watchdog timer 2 operation   */  } <1>
```

Section of main processing

Main processing for other than WDT2 is omitted here

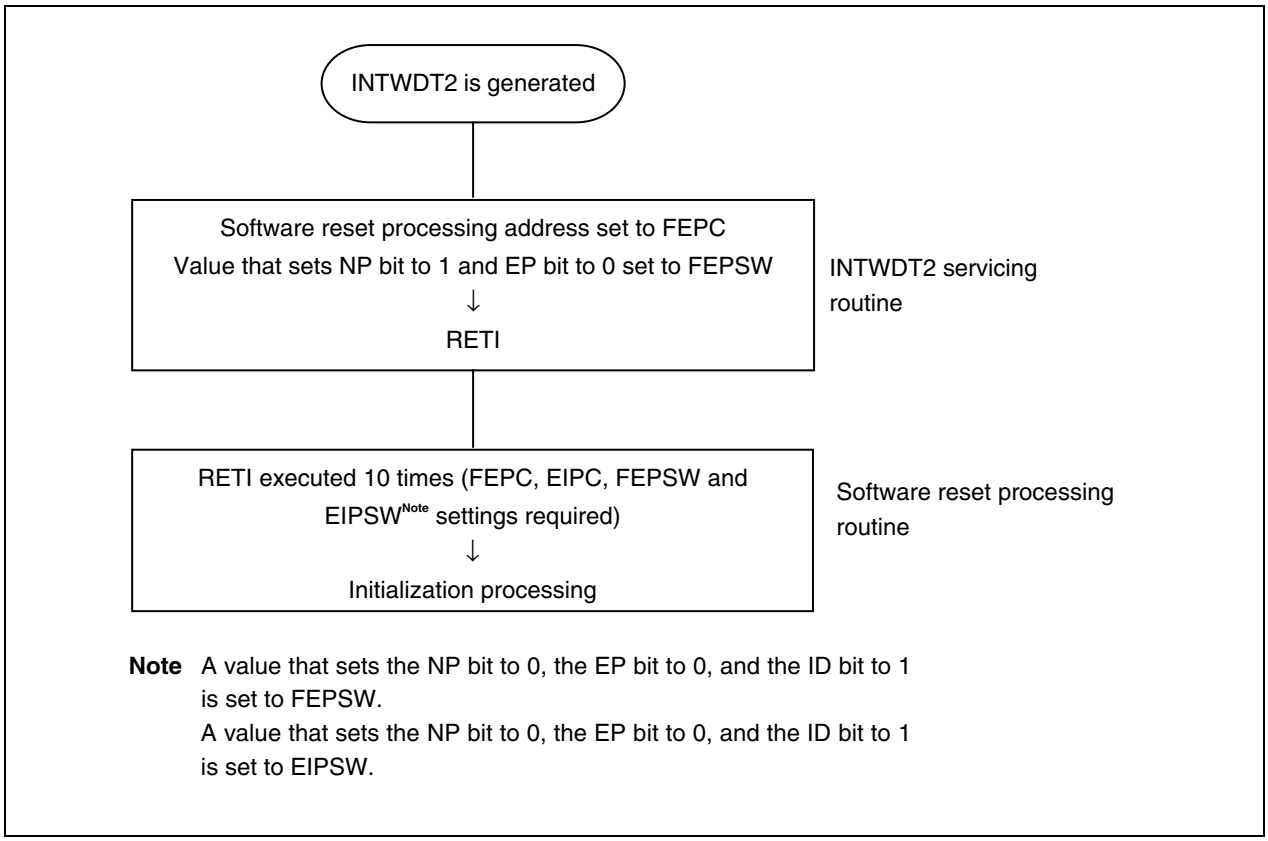
```
WDTE = 0xAC;                    /* Clears WDT2 count                   */  } <2>
```

- Using the detection of a watchdog timer 2 overflow as a trigger to generate an interrupt

  The overflow of watchdog timer 2 is likely to cause the CPU to enter an infinite processing loop. It is therefore recommended to set watchdog timer 2 to the reset mode (by setting the WDM21 bit to 1) so that the CPU is reset when WDT2 overflows.

  If you choose to set watchdog timer 2 to non-maskable interrupt request mode (by setting the WDM21 bit to 0 and the WDM20 bit to 1), however, be sure to stop the system after the system error processing has been completed by the INTWDT2 interrupt servicing routine. The system cannot be returned to the main processing routine by using the RETI instruction after the servicing of a non-maskable interrupt generated by the INTWDT2 signal has finished. To return the system to the main processing routine following the servicing of an INTWDT2 interrupt, execute the software reset processing shown below.

  Note that in this software reset processing, registers that can be set only once following the release of reset (such as the WDTM2 register) cannot be set again. These registers must be initialized by executing a hardware reset by means such as inputting a signal to the reset pin.



Note A value that sets the NP bit to 0, the EP bit to 0, and the ID bit to 1 is set to FEPSW.
A value that sets the NP bit to 0, the EP bit to 0, and the ID bit to 1 is set to EIPSW.

• Example of program

```
#*******************************************#
#       Interrupt initialization processing   #
#*******************************************#
        .global _initint

_initint:
        mov     initloop1,r6    -- Sets the processing routine address
        ldsr    r6,2            -- Set to FEPC
        mov     0xa0,r6         -- NP=1, EP=0
        ldsr    r6,3            -- Set to FEPSW
        reti                    -- Processing restored from NMI and returned to initloop1



initloop1:
        mov     0x20,r6         -- PSW.NP set to 0 by next RETI instruction
        ldsr    r6,3            -- Set to FEPSW
        ldsr    r6,1            -- Set to EIPSW
        mov     initloop2,r6    -- Sets processing routine address 2
        ldsr    r6,2            -- Set to FEPC
        ldsr    r6,0            -- Set to EIPC
        mov     0x0b,r6         -- Count initial value (10 times)
        reti

initloop2:
        sub     1,r6            -- Loop count (-1)
        bz      initend         -- End of interrupt initialization
        reti

initend:
```

4.2 Checking Detection of WDT2 Reset

When a WDT2 reset occurs, the WDT2RF bit of the reset source flag register (RESF) is set. On the other hand, when a reset is generated by an input to the RESET pin, the WDT2RF bit is cleared. Therefore, by checking the WDT2RF bit after the reset is released, it is possible to ascertain whether the reset source was an WDT2 reset or an input to the RESET pin.

4.2.1 Reset source flag register (RESF)

The RESF register stores information on which reset signal—the reset signal from which source—generated a reset.

This register can be read or written in 8-bit or 1-bit units.

Note, however, that the RESF register can only be written using a combination of specific sequences.

A reset generated by an input to the $\overline{\text{RESET}}$ pin sets this register to 0x00. A reset generated by any other source, such as watchdog timer 2 (WDT2), the low-voltage detector (LVI), or the clock monitor (CLM), sets the flag of the corresponding source (WDT2RF, CLMRF, LVIRF bits); the other source flags hold their previous values.

Figure 4-3. Format of RESF Register

Reset source flag register (RESF)
Address: 0xFFFFF888

7	6	5	4	3	2	1	0
0	0	0	WDT2RF	0	0	CLMRF	LVIRF

WDT2RF	Occurrence of reset signal from WDT2
0	Did not occur
1	Occurred

CLMRF	Occurrence of reset signal from CLM
0	Did not occur
1	Occurred

LVIRF	Occurrence of reset signal from LVI
0	Did not occur
1	Occurred

Notes 1. Only 0 can be written to each bit. If writing 0 conflicts with the flag being set (due to the occurrence of a reset), flag setting takes precedence.

2. If watchdog timer 2 (WDT2), the low-voltage detector (LVI), and the clock monitor (CLM) are being used at the same time, the relevant reset source flag must be cleared after checking the reset source.

Remark The blue values indicate the bits to be checked in the sample program.

[Clearing the reset source flag]
As mentioned in Note 2 on the previous page, there are cases when the reset source flag has to be cleared after checking the reset source. In this sample program, however, the reset source flag does not have to be cleared because only the watchdog timer 2 (WDT2) is used.

CHAPTER 5 RELATED DOCUMENTS

Document	English
V850ES/JF3-L Hardware User's Manual	PDF
V850ES/JG3-L Hardware User's Manual	PDF
PM+ Ver.6.30 User's Manual	PDF
CA850 Ver.3.20 C Compiler Package Operation User's Manual	PDF
CA850 Ver.3.20 C Compiler Package C Language User's Manual	PDF
CA850 Ver.3.20 C Compiler Package Assembly Language User's Manual	PDF
CA850 Ver.3.20 C Compiler Package Link Directive User's Manual	PDF
V850ES Architecture User's Manual	PDF
QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual	PDF
ID850QB Ver. 3.40 Integrated Debugger Operation User's Manual	PDF

APPENDIX A PROGRAM LIST

The V850ES/Jx3-L microcontroller source program is shown below as a program list example.

- opt_b.s

```
#-------------------------------------------------------------------------------
#
#    NEC Electronics     V850ES/Jx3-L microcontroller
#
#-------------------------------------------------------------------------------
#    V850ES/JG3-L JF3-L  JF3-L sample program
#-------------------------------------------------------------------------------
#    Reset Generation When Infinite Loop Detected
#-------------------------------------------------------------------------------
#[History]
#    2008.11.--   Released
#-------------------------------------------------------------------------------
#[Overview]
#    This sample program sets the option byte.
#-------------------------------------------------------------------------------

     .section "OPTION_BYTES"
     .byte 0b00000101 -- 0x7a (5 MHz: Sets the oscillation stabilization time to 6.554 ms.)
     .byte 0b00000000 -- 0x7b            ↑
     .byte 0b00000000 -- 0x7c            ↑
     .byte 0b00000000 -- 0x7d 0x00 must be set to addresses 0x7b to 0x7f.
     .byte 0b00000000 -- 0x7e            ↓
     .byte 0b00000000 -- 0x7f            ↓
```

● minicube2.s

```
#-------------------------------------------------------------------------------
#
#    NEC Electronics     V850ES/Jx3-L microcontroller
#
#-------------------------------------------------------------------------------
#    V850ES/JG3-L JF3-L sample program
#-------------------------------------------------------------------------------
#    Reset Generation When Infinite Loop Detected
#-------------------------------------------------------------------------------
#[History]
#    2008.11.--   Released
#-------------------------------------------------------------------------------
#[Overview]
#    This sample program secures the resources required when using MINICUBE2.
#       (Example of using MINICUBE2 via CSIB0)
#-------------------------------------------------------------------------------

     -- Securing a 2 KB space as the monitor ROM section
     .section "MonitorROM", const
     .space 0x800, 0xff

     -- Securing an interrupt vector for debugging
     .section "DBG0"
     .space 4, 0xff

     -- Securing a reception interrupt vector for serial communication
     .section "INTCB0R"
     .space 4, 0xff

     -- Securing a 16-byte space as the monitor RAM section
     .section "MonitorRAM", bss
     .lcomm monitorramsym, 16, 4
```

● AppNote_INT.dir

```
#   Sample link directive file (not use RTOS/use internal memory only)
#
#   Copyright (C) NEC Electronics Corporation 2002
#   All rights reserved by NEC Electronics Corporation.
#
#   This is a sample file.
#   NEC Electronics assumes no responsibility for any losses incurred by
#   customers or third parties arising from the use of this file.
#
#   Generated      : PM+ V6.31  [ 9 Jul 2007]
#   Sample Version : E1.00b [12 Jun 2002]
#   Device         : uPD70F3738 (C:\Program Files\NEC Electronics
#   Tools\DEV\DF3738.800)
#   Internal RAM   : 0x3ffb000 - 0x3ffefff
#
#   NOTICE:
#        Allocation of SCONST, CONST and TEXT depends on the user program.
#
#        If interrupt handler(s) are specified in the user program then
#        the interrupt handler(s) are allocated from address 0 and
#        SCONST, CONST and TEXT are allocated after the interrupt handler(s).

SCONST  : !LOAD ?R {
        .sconst         = $PROGBITS     ?A .sconst;
};

CONST   : !LOAD ?R {
        .const          = $PROGBITS     ?A .const;
};

TEXT    : !LOAD ?RX {
        .pro_epi_runtime = $PROGBITS    ?AX .pro_epi_runtime;
        .text            = $PROGBITS    ?AX .text;
};

### For MINICUBE2###
MROMSEG : !LOAD ?R V0x03F800{
       MonitorROM = $PROGBITS ?A MonitorROM;
};
```

0x01F800 for products with 128 KB internal ROM

Difference from the default link directive file (additional code)

A reserved area for MINICUBE2 is secured.

```
SIDATA  : !LOAD ?RW V0x3ffb000 {
        .tidata.byte    = $PROGBITS     ?AW .tidata.byte;
        .tibss.byte     = $NOBITS       ?AW .tibss.byte;
        .tidata.word    = $PROGBITS     ?AW .tidata.word;
        .tibss.word     = $NOBITS       ?AW .tibss.word;
        .tidata         = $PROGBITS     ?AW .tidata;
        .tibss          = $NOBITS       ?AW .tibss;
        .sidata         = $PROGBITS     ?AW .sidata;
        .sibss          = $NOBITS       ?AW .sibss;
};

DATA    : !LOAD ?RW V0x3ffb100 {
        .data           = $PROGBITS     ?AW  .data;
        .sdata          = $PROGBITS     ?AWG .sdata;
        .sbss           = $NOBITS       ?AWG .sbss;
        .bss            = $NOBITS       ?AW  .bss;
};
```

```
### For MINICUBE2 ###
MRAMSEG : !LOAD ?RW V0x03FFEFF0{
        MonitorRAM = $NOBITS ?AW MonitorRAM;
};
```

Difference from the default link directive file (additional code)

A reserved area for MINICUBE2 is secured.

```
__tp_TEXT @ %TP_SYMBOL;
__gp_DATA @ %GP_SYMBOL &__tp_TEXT{DATA};
__ep_DATA @ %EP_SYMBOL;
```

● main.c

```
/*---------------------------------------------------------------------------*/
/*
/*  NEC Electronics     V850ES/Jx3-L microcontroller
/*
/*---------------------------------------------------------------------------*/
/*  V850ES/JG3-L sample program
/*---------------------------------------------------------------------------*/
/*  Reset Generation When Infinite Loop Detected
/*---------------------------------------------------------------------------*/
/*[History]
/*  2008.11.--  Released
/*---------------------------------------------------------------------------*/
/*[Overview]
/*  This sample program presents an example of using the watchdog timer 2 (WDT2).
/*  The WDT2 overflow time is set to 125 ms and an internal reset signal
/*  (WDT2RES) is generated when an overflow occurs.
/*  After initial setup is complete, interrupts are generated and serviced upon
/*  detection of the falling edge of the switch input. While the switch is being
/*  pressed, LED1 blinks in a cycle of 55 ms and the count of WDT2 is cleared.
/*  When a reset is generated by WDT2, the initial settings specify that LED2
/*  turns on.
/*
/*
/*  Among the peripheral functions that are stopped after reset is released,
/*  those that are not used in this sample program are not set.
/*
/*
/* <Main setting contents>
/*  • Using pragma directives to enable setting the interrupt handler and
/*    describing peripheral I/O register names
/*  • Defining a wait adjustment value of 10 ms for chattering
/*  • Defining the LED1 blinking time to be set to TMM0 (120 ms, 55 ms)
/*  • Performing prototype definitions
/*  • Setting a bus wait for on-chip peripheral I/O registers, starting the WDT2
      operation, and setting the clock
/*  • Initializing unused ports
/*  • Initializing external interrupt ports (falling edge) and LED output ports
/*  • The TMM0 compare match interrupt request flag is monitored and when an
/*    interrupt request occurs, the WDT2 count is cleared, the output of LED1 is
/*    inverted, and the TMM0 compare match interrupt request flag is cleared.
/* <Interrupt servicing>
/*  • The LED1 blinking cycle is set to 55 ms.
/*  • The TMM0 compare match interrupt request flag is monitored and when an
      interrupt request occurs, the WDT2 count is cleared, the output of LED1 is
      inverted, and the TMM0 compare match interrupt request flag is cleared.
```

```
/*  • When the switch is off, the WDT2 count is cleared, and the LED1 blinking
/*    cycle is set to 120 ms.
/*   (Chattering elimination time during switch input: 10 ms)
/*
/*
/*[I/O port settings]
/*
/* Input port      : P03(INTP0)
/* Output ports    : PCM2, PCM3
/* Unused ports    : P02, P04 to P06, P10 and P11, P30 to P39, P50 to P55, P70 to
/*                   P711,  P90 to P915, PCM0 and PCM1, PCT0, PCT1, PCT4, PCT6,
/*                   PDH0 to PDH5, PDL0 to PDL15
/*                   *Preset all unused ports as output ports (low-level output).
/*
/*---------------------------------------------------------------------------*/


/*---------------------------*/
/*   pragma directives     */
/*---------------------------*/
#pragma ioreg                       /* Enables describing to peripheral I/O
                                       registers.                              */
#pragma interrupt INTP0 f_int_intp0 /* Specifies the interrupt handler.        */



/*---------------------------*/
/* Constant definitions    */
/*---------------------------*/
#define LIMIT_10ms_WAIT    (28391)  /* Defines the constant for a 10 ms wait adjustment. */
#define VAL_55ms_CNT       (2149)   /* LED1 blinking cycle (55 ms)                       */
#define VAL_120ms_CNT      (4688)   /* LED1 blinking cycle (120 ms)                      */
/*---------------------------*/
/*  Prototype definitions  */
/*---------------------------*/
static void f_init( void );              /* Initialization function                  */
static void f_init_clk_bus_wdt2( void ); /* Clock bus WDT2 initialization function   */
static void f_init_port_func( void );    /* Port/alternate-function initialization
                                            function                                */
static void f_init_int_tmm( void );      /* TMM0 initialization function            */
```

```
/*********************************/
/*      Main module          */
/*********************************/
void main( void )
{
        f_init();                       /* Executes initialization.                        */

        __EI();                         /* Enables interrupts.                             */

        while( 1 )                      /* Main loop (infinite loop)                       */
        {
               if ( TM0EQIF0 == 1 )     /* Is there an INTTM0EQ0 interrupt request signal? */
               {
                        WDTE = 0xAC;    /* Clears the WDT2 count.                          */
                        PCM.3 ^= 1;     /* Inverts the LED1 output.                        */
                        TM0EQIF0 = 0;   /* Clears the TMM0 compare match interrupt request.*/
               }
        }

        return;
}


/*---------------------------*/
/*  Initialization module  */
/*---------------------------*/
static void f_init( void )
{
        f_init_clk_bus_wdt2();          /* Sets a bus wait for on-chip peripheral I/O
                                           registers, stops WDT2, and sets the clock.      */

        f_init_port_func();             /* Sets the port/alternate function.               */

        f_init_int_tmm();               /* Sets the TMM0 timer.                            */

        return;
}
```

```
/*--------------------------------------*/
/* Initializing clock/bus wait/WDT2 */
/*--------------------------------------*/
static void f_init_clk_bus_wdt2( void )
{
       VSWC   = 0x01;                /* Sets a bus wait for on-chip
                                        peripheral I/O registers.              */

                                     /* Specifies normal operation mode for OCDM. */
#pragma asm
       st.b   r0, PRCMD
       st.b   r0, OCDM
#pragma endasm
```

Note that accessing a specific register must be described using an assembler.

```
       RSTOP  = 1;                   /* Stops the internal oscillator.          */
       WDTM2  = 0x5B;                /* Starts the operation of watchdog timer 2  */

                                     /* Sets not to divide the clock.           */
                                     /* Sets the use of the subclock            */
#pragma asm
       st.b   r0, PRCMD
       st.b   r0, PCC
#pragma endasm

      PLLCTL = 0x03;                 /* Sets to PLL mode.                       */

      return;
}
```

```
/*---------------------------------------*/
/*  Setting the port/alternate function  */
/*---------------------------------------*/
static void f_init_port_func( void )
{
        P0     = 0x00;                      /* Sets P02 to P06 to output low level.  */
        PM0    = 0x8B;                      /* Connects P03 to an input latch        */
        PMC0   = 0x08;                      /* Sets P03 to INTP0 input               */

        P1     = 0x00;                      /* Sets P10 and P11 to output low level. */
        PM1    = 0xFC;
        P3     = 0x0000;                    /* Sets P30 to P39 to output low level.  */
        PM3    = 0xFC00;
        PMC3   = 0x0000;

#if(0)  /* To use P4 as CSIB0 when using MINICUBE2,                    */
        /* P4 is not initialized as an unused pin (QB-V850ESJG3L-TB) */
        P4     = 0x00;              /* Sets P40 to P42 to output low level.          */
        PM4    = 0xF8;
        PMC4   = 0x00;
#endif

        P5     = 0x00;              /* Sets P50 to P55 to output low level.          */
        PM5    = 0xC0;
        PMC5   = 0x00;

        P7H    = 0x00;              /* Sets P70 and P711 to output low level.        */
        P7L    = 0x00;
        PM7H   = 0xF0;
        PM7L   = 0x00;

        P9     = 0x0000;            /* Sets P90 to P915 to output low level.         */
        PM9    = 0x0000;
        PMC9   = 0x0000;
```

With V850ES/JF3-L, the setting value is 0xFE.

With V850ES/JF3-L, only P10 is set.

With V850ES/JF3-L, the setting value is 0xFCC0.

With V850ES/JF3-L, P30 to P35, P38, and P39 are set.

With V850ES/JF3-L, these are not set because the registers do not exist.

With V850ES/JF3-L, P70 to P77 are set.

With V850ES/JF3-L, the setting value is 0x1C3C.

With V850ES/JF3-L, P90, P91, P96 to P99, and P913 to P915 are set.

```
        PCM    = 0x0C;          /* Sets PCM0 and PCM1 to output low level and values
        to turn off the LEDs to PCM2 and PCM3                                    */
        if( RESF.4 == 1 )
        {
                PCM = 0x08;     /* Sets that LED2 is turned on when the reset
                                   source is WDT2                                */
        }
        PMCM   = 0xF0;
        PMCCM  = 0x00;

        PCT    = 0x00;              /* Sets PCT0, 1, 4, and 6 to output low level.  */
        PMCT   = 0xAC;
        PMCCT  = 0x00;

        PDH    = 0x00;              /* Sets PDH0 to PDH5 to output low level.       */
        PMDH   = 0xC0;
        PMCDH  = 0x00;

        PDL    = 0x0000;            /* Sets PDL0 to PDL15 to output low level. */
        PMDL   = 0x0000;
        PMCDL  = 0x0000;

        /* Setting the interrupt function */
        INTF0  = 0x08;              /* Specifies the falling edge of INTP0.         */
        INTR0  = 0x00;              /* ↓                                            */
        PIC0   = 0x07;              /* Sets the priority of INTP0 to level 7
                                       and unmasks INTP0.                        */

    return;
}


/*---------------------------*/
/*     Setting timer M     */
/*---------------------------*/
static void f_init_int_tmm( void )
{
        TM0CTL0 = 0x04;             /* Disables TMM0 operation.                     */
                                    /* Count clock = fxx/512                        */
        TM0CMP0 = VAL_120ms_CNT;    /* Sets TMM0 count.                             */
        TM0EQMK0 = 1;               /* Masks timer M interrupts.                    */
        TM0CE = 1;                  /* Enables TMM0 operation.                      */
}
```

With V850ES/JF3-L, the setting value is 0xFC.

With V850ES/JF3-L, PDH0 and PDH1 are set.

```
/*******************************/
/*     Interrupt module        */
/*******************************/
__interrupt
void f_int_intp0( void )
{
       unsigned int loop_wait;                /* for loop counter                */

       /* 10 ms wait to eliminate chattering */
       for( loop_wait = 0 ; loop_wait < LIMIT_10ms_WAIT ; loop_wait++ )
       {
              __nop();
       }

       if( ( P0 & 0x08 ) == 0x00 )            /* Identifies that SW1 has been
                                                 pressed after the wait.         */
       {
              /* SW ON        */
              TM0CE = 0;                      /* Stops the count operation.      */
              TM0CMP0 = VAL_55ms_CNT;         /* Sets the LED1 blinking cycle to
                                                 55 ms.                          */
              TM0EQIF0 = 0;                   /* Clears the TMM0 compare match
                                                 interrupt request.              */
              TM0CE = 1;                      /* Starts the count operation.     */
              while ( ( P0 & 0x08 ) == 0x00 )
              {
                     if ( TM0EQIF0 == 1 )     /* Is there an interrupt request
                                                 signal?                         */
                     {
                            WDTE = 0xAC;      /* Clears the WDT2 count.          */
                            PCM.3 ^= 1;       /* Inverts the LED1 output.        */
                            TM0EQIF0 = 0;     /* Clears the TMM0 compare match
                                                 interrupt request.              */
                     }
              }
              /* SW OFF      */
              WDTE = 0xAC;                    /* Clears the WDT2 counter.        */
              TM0CE = 0;                      /* Stops the count operation.      */
              TM0CMP0 = VAL_120ms_CNT;        /* Sets the LED1 blinking cycle to
                                                 120 ms.                         */
              TM0CE = 1;                      /* Starts the count operation.     */
       }

       PIF0 = 0;
                                              /* Failsafe: Multiple requests
                                                 Cleared.                        */

       return;                                /* Processing moves to reti,
                                                 depending on the _interrupt
                                                 modifier.                       */
}
```

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